The following Listing of Claims will replace all prior versions, and listings, of claims in the present application:

Listing of Claims:

1. (Previously presented) A method for making a dielectric structure for dual-damascene applications, the method comprising:

providing a substrate;

fabricating metallization lines within the substrate;

forming a barrier layer over the metallization lines and the substrate;

forming an inorganic dielectric layer to a thickness of between about 0.4 microns (μ) and 0.5 microns to define a via dielectric layer directly over the barrier layer, the inorganic dielectric layer having a dielectric constant of about 4 and being highly selective relative to the barrier layer when etched; and

forming a carbon doped oxide layer to a thickness of between about 0.5 microns and 0.6 microns to define a trench dielectric layer over and in direct contact with the inorganic dielectric layer, the trench layer being formed to define a metallization line layer.

2. (Previously Presented) A method for making a dielectric structure for dual-damascene applications as recited in claim 1, further comprising:

forming a trench in the carbon doped oxide layer using a first etch chemistry.

3. (Original) A method for making a dielectric structure for dual-damascene applications as recited in claim 2, further comprising:

forming a via in the inorganic dielectric layer using a second etch chemistry, the second etch chemistry being different than the first etch chemistry and the via being within the trench.

4. (Original) A method for making a dielectric structure for dual-damascene applications as recited in claim 1, wherein the barrier layer is one of a silicon nitride layer and a silicon carbide layer.

5. (Original) A method for making a dielectric structure for dual-damascene applications as recited in claim 4, wherein the forming of the inorganic dielectric layer includes,

depositing a TEOS silicon dioxide material over the barrier layer.

6. (Previously Presented) A method for making a dielectric structure for dual-damascene applications as recited in claim 5, wherein the carbon doped oxide layer is a low dielectric constant layer having a dielectric constant of about and no greater than 3.0.

7. (Previously Presented) A method for making a dielectric structure for dual-damascene applications as recited in claim 3, wherein the inorganic dielectric layer is one of a TEOS oxide layer and a fluorine doped oxide layer.

8. (Original) A method for making a dielectric structure for dual-damascene applications as recited in claim 7, wherein the first etch chemistry is optimized to etch through the carbon doped oxide layer and the second etch chemistry is optimized to etch through the TEOS oxide layer or the fluorine doped oxide layer.

9. (Original) A method for making a dielectric structure for dual-damascene applications as recited in claim 8, wherein the second etch chemistry is selective to the barrier layer.

10. (Previously presented) A method for making a multi-layer inter-metal dielectric over a substrate, comprising:

forming a barrier layer over the substrate;

forming a silicon dioxide layer over the barrier layer, the silicon dioxide layer having a thickness between about 0.4 microns (μ) and 0.5 microns and a dielectric constant of about 4;

forming a carbon doped oxide layer directly over and in direct contact with the silicon dioxide layer, the carbon doped oxide layer ranging between about 0.5 microns and 0.6 microns in thickness;

forming a trench through the carbon doped oxide layer; and

forming a via in the trench extending through the silicon dioxide layer to the barrier layer,

wherein the silicon dioxide layer defines a via layer and the carbon doped oxide layer defines a trench layer for metallization lines.

11. (Original) A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 10, wherein the barrier layer is one of a silicon nitride layer and a silicon carbide layer.

12. (Original) A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 11, wherein the forming of the silicon dioxide layer includes,

depositing one of an un-doped TEOS oxide layer and a fluorine doped oxide layer.

13. (Previously Presented) A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 12, wherein the carbon doped oxide layer is a low dielectric constant layer having a dielectric constant less than or equal to about 3.0.

14. (Previously Presented) A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 10, wherein forming the via in the trench extending to the barrier layer further includes,

implementing a first chemistry optimized to etch through the carbon doped oxide layer; and

implementing a second chemistry which is different than the first etch chemistry and is optimized to etch through the silicon dioxide layer.

15. (Original) A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 14, wherein the second chemistry that is optimized to etch through the silicon dioxide layer is selective to the barrier layer.

16. (Original) A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 15, wherein the barrier layer is one of a silicon nitride layer and a silicon carbide layer.

17-25. (Canceled)

26. (Original) A method for making a multi-layer intermetal dielectric over a substrate as recited in claim 10, further comprising:

etching the barrier layer; and

forming a via and trench barrier layer to cover a surface within the via and the trench,

wherein the via and trench barrier layer is one of tantalum nitride material and tantalum material.

27-31. (Canceled)

32. (Withdrawn) A method for making an inter-metal dielectric structure for dual damascene applications, comprising:

providing a substrate, the substrate having metallization lines with conductive material disposed therein;

forming a barrier over the substrate;

forming a via dielectric layer directly over the barrier, the via dielectric layer being formed of an inorganic silicon dioxide having a dielectric constant of about 4.0 and having a via dielectric thickness of between 0.4 microns (μ) and 0.5 microns and being highly selective to the barrier when etched;

forming a trench dielectric layer over and in direct contact with the via dielectric layer, the trench dielectric layer being formed of a low k dielectric material having a dielectric constant of less than or equal to about 3.0 and having a trench dielectric thickness of between 0.5 microns and 0.6 microns;

forming a trench in the trench dielectric layer using a first etch chemistry;

forming a via in the via dielectric layer using a second etch chemistry, the second etch chemistry being optimized to etch the inorganic silicon dioxide having the dielectric constant of about 4.0 and being highly selective to the barrier;

removing a portion of the barrier layer within the via;

forming a feature barrier within the surfaces of the trench and the via; and

depositing copper within the via and the trench over the feature barrier,

wherein the barrier layer is formed of one of silicon nitride and silicon carbide.